WHAT WE CLAIM ARE:

1. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film formed on a partial area of a surface of said semiconductor substrate;

a gate electrode formed on said gate insulating film;

a lamination film formed on a side wall of said gate electrode and on the surface of said semiconductor substrate on both sides of said gate electrode, conformable to the side walls and the surface, said lamination film having a structure of at least three layers, each of the three layers being made of insulating material, and a middle layer being made of material easier to trap carriers than other two layers;

a side wall spacer made of conductive material and facing the side wall of said gate electrode and the surface of said semiconductor substrate via said lamination film;

a conductive connection member electrically connecting said side wall spacer and said gate electrode; and

impurity doped regions formed in a surface layer of said semiconductor substrate in areas sandwiching said gate electrode along a first direction parallel to the surface of said semiconductor substrate, edges of said impurity doped regions being disposed under said lamination film to some depth and not reaching boundaries of said gate electrode.

2. A semiconductor device according to claim 1, further comprising:

a first insulating film formed on surfaces of said impurity doped regions, said first insulating film extending along an interface between said

lamination film and said impurity doped regions to a depth shallower than boundaries of said impurity doped regions and being thicker than a layer of said lamination film nearest to said semiconductor substrate,

wherein said connection member extends to a surface of said first insulating film.

3. A semiconductor device according to claim 1, wherein:

said side wall spacer projects higher than an upper surface of said gate electrode and a top of said lamination film;

the semiconductor device further comprises a second insulating film formed on surfaces of said impurity doped regions in tight contact with outer side walls of said side wall spacer; and

said connection member is in contact with inner walls of said wall spacer in an area projecting higher than said lamination film and in contact with an upper surface of said gate electrode.

4. A semiconductor device according to claim 3, wherein said connection member extends to an upper surface of said second insulating film.

5. A semiconductor device comprising:

a semiconductor substrate;

a plurality of impurity doped regions of a first conductivity type formed in a surface layer of said semiconductor substrate, extending in a first direction and disposed in parallel to each other;

a plurality of gate lines disposed on said semiconductor substrate, extending in a second direction crossing the first direction and disposed in

parallel to each other at some interval, said gate line being insulated from said impurity doped region in each cross point between said gate line and said impurity doped region;

a FET disposed in each cross point between a pair of adjacent impurity doped regions and said gate line; and

a channel stopper region of a second conductivity type opposite to the first conductivity type, said channel stopper region being formed in the surface layer of said semiconductor substrate between channel regions of two FET's juxtaposed in the first direction,

wherein each of said FET's comprises:

the channel region between a corresponding pair of impurity doped regions;

a gate insulating film formed on the channel region and spaced apart by some distance from the corresponding pair of impurity doped regions;

a gate electrode formed on said gate insulating film and connected to a corresponding gate line;

a lamination film conformably covering a side wall of said gate electrode and a surface of said semiconductor substrate between each impurity doped region of the corresponding pair of impurity doped regions and said gate electrode, said lamination film having a structure of at least three layers, a middle layer being made of material easier to trap carriers than other two layers;

a side wall spacer made of conductive material, facing the side wall of said gate electrode and the channel region via said lamination film, and connected to a corresponding gate line.

6. A semiconductor device according to claim 5, wherein:

an edge of each of said impurity doped regions is disposed under a corresponding lamination film; and

the semiconductor device further comprises a first insulating film disposed between said impurity doped region and said gate line at a cross point therebetween, said first insulating film being disposed along an interface between said lamination film and said impurity doped region to a depth shallower than boundary of said impurity doped region and being thicker than a layer of said lamination film nearest to said semiconductor substrate.

7. A semiconductor device according to claim 5, further comprises:

a second insulating film disposed between said impurity doped region and said gate line at a cross point therebetween, said second insulating film being in tight contact with an outer side wall of said side wall spacer,

wherein said side wall spacer project higher than an upper surface of said gate electrode and a top of said lamination film, and each of said gate lines is in contact with an inner wall of projected portion of a corresponding side wall spacer and the top surface of a corresponding gate electrode.

8. A method of manufacturing a semiconductor device, comprising the steps of:

forming two layers of a gate insulating film and a gate electrode on a partial area of a surface of a semiconductor substrate;

forming a lamination film on surfaces of the semiconductor substrate, gate insulating film and gate electrode conformable to the surfaces, the lamination film having a structure of at least three layers, each of the three layers being made of insulating material, and a middle layer being made of material easier to trap carriers than other two layers;

forming a conductive side wall spacer on a surface of the lamination film in areas along a side wall of the gate electrode;

etching the lamination film at least to a bottom of the middle layer in an area not covered with the side wall spacers;

implanting first impurities into a surface layer of the semiconductor substrate by using the gate electrode and the side wall spacer as a mask;

forming a first insulating film by locally oxidizing the surface of the semiconductor substrate not covered with the gate electrode and the side wall spacer;

removing an insulating film formed on an upper surface of the gate electrode and on a surface of the side wall spacer; and

forming a connection member electrically connecting the upper surface of the gate electrode and the surface of the side wall spacer.

9. A method according to claim 8, wherein:

a two-layer structure of the gate insulating film and gate electrode extends in a first direction on the surface of the semiconductor substrate and is formed in each of a plurality of areas disposed in parallel to each other; and

said step of forming the connection member comprises:

a step of covering a whole surface of the semiconductor substrate with a conductive film;

a step of patterning the conductive film to leave a plurality of gate lines extending in a second direction crossing the first direction and disposed in parallel to each other;

a step of etching the gate electrode by using the gate lines as a mask after the gate lines are left; and

a step of implanting second impurities of a conductivity type opposite to the first impurities into a surface layer of the semiconductor substrate under an area where the gate electrode was etched.

10. A method of manufacturing a semiconductor device, comprising the steps of:

forming three layers of a gate insulating film, a gate electrode and a gate upper film on a partial area of a surface of a semiconductor substrate;

forming a lamination film of a lower layer, a middle layer and an upper layer, the lower layer covering exposed surfaces of at least the semiconductor substrate, gate insulating film and gate electrode, the middle layer covering surfaces of the lower layer and gate upper film, the upper layer covering the middle layer, each of the lower, middle and upper layers being made of insulating material, and the middle layer being made of material easier to trap carriers than the lower and upper layers;

forming a first conductive film covering a surface of the lamination film;

anisotropically etching the lamination film and first film to leave a side wall spacer, which is made of a portion of the first film, and a portion of the lamination film on a side wall of the gate electrode and gate upper film, and to remove at least the first film and the upper and middle layers of the lamination film on the surface of the semiconductor substrate in an area where the gate electrode is not disposed;

implanting first impurities into a surface layer of the semiconductor substrate by using the gate electrode, gate upper film and side wall spacer as a mask;

forming a second film of insulating material on or over a whole surface of the semiconductor substrate;

polishing the second film until the gate upper film is exposed;

removing the gate upper film and the lamination film left on the side wall of the gate upper film; and

forming a connection member electrically connecting an upper surface of the gate electrode and an exposed surface of the side wall spacer.

11. A method according to claim 10, wherein:

a three-layer structure of the gate insulating film, gate electrode and gate upper film extends in a first direction on the surface of the semiconductor substrate and is formed on each of a plurality of areas disposed in parallel to each other; and

said step of forming the connection member comprises:

a step of covering a whole surface of the semiconductor substrate with a third conductive film;

a step of patterning the third film to leave a plurality of gate lines extending in a second direction crossing the first direction and disposed in parallel to each other;

a step of etching the gate electrode, at least an upper layer of the second film and the side wall spacer by using the gate lines as a mask after the gate lines are left; and

a step of implanting second impurities of a conductivity type opposite to the first impurities into a surface layer of the semiconductor substrate under an area where the gate electrode was etched.

12. A semiconductor device comprising:

a gate insulating film formed on a channel region defined in a surface layer of a semiconductor substrate;

source and drain regions formed in the surface layer in both side areas of the channel region;

carrier trap films covering first and second areas and made of material easier to trap carriers than the gate insulating film, an upper surface of the gate insulating film having the first area on the source region side, the second area on the drain region side and a third area between the first and second areas;

a coating film made of insulating material and covering surfaces of the carrier trap films; and

a gate electrode continuously covering at least a surface from a boundary between the source region and channel region to a boundary between the drain region and channel region among surfaces of the coating film and the gate insulating film on the third area.

13. A semiconductor device comprising:

a semiconductor substrate;

a plurality of impurity doped regions of a first conductivity type formed in a surface layer of said semiconductor substrate, extending in a first direction and disposed in parallel to each other;

a plurality of gate lines disposed on or over said semiconductor substrate, extending in a second direction crossing the first direction and disposed in parallel to each other at some interval, said gate line being insulated from said impurity doped region at each cross point between said gate

line and said impurity doped region;

a FET disposed at each cross point between a pair of adjacent impurity doped regions and said gate line; and

a channel stopper region of a second conductivity type opposite to the first conductivity type, said channel stopper region being formed in the surface layer of said semiconductor substrate between channel regions of two FET's juxtaposed in the first direction,

wherein each of said FET's comprises:

the channel region between a corresponding pair of impurity doped regions;

a gate insulating film formed on the channel region;

carrier trap films covering first and second areas and made of material easier to trap carriers than the gate insulating film, an upper surface of the gate insulating film having the first area on one side of the corresponding pair of impurity doped regions, the second area on the other side, and a third area between the first and second areas; and

a coating film made of insulating material and covering surfaces of the carrier trap films,

wherein the gate line covers the third area of the gate insulating film of a corresponding FET and the coating film and serves also as a gate electrode of FET.

14. A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a gate insulating film, a carrier trap film made of material easier to trap carriers than the gate insulating film, and an upper

insulating film on a surface of a semiconductor substrate;

forming resist patterns on or over the surface of the semiconductor substrate, the resist patterns covering surfaces of the upper insulating films formed in a pair of elongated first channel regions disposed in parallel to each other and spaced apart by some distance;

etching the upper insulating film and carrier trap film by using the resist patterns as a mask;

implanting impurity ions into a surface layer of the semiconductor substrate under conditions that an area between the pair of resist patterns is shaded by one of the resist patterns so that impurity ions are not implanted into the shaded area, and that in each of areas outside of the pair of resist patterns, boundaries of the ion implanted areas become coincident with boundaries of the resist patterns or extends from the boundaries of the resist pattern to an inside region;

removing the resist patterns;

forming a first film made of insulating material on the surface layer of the semiconductor substrate in the area implanted with ions by said impurity ion implanting step; and

forming a gate electrode on the upper insulating films covering the carrier trap films over the pair of first channel regions and on the gate insulating film between the pair of first channel regions.

15. A semiconductor device comprising:

source and drain regions formed in a surface layer of a semiconductor substrate and spaced apart by some distance;

an intermediate region formed in the surface layer between said

source and drain regions, spaced apart by some distance from both said source and drain regions, and doped with impurities of the same conductivity type as said source and drain regions;

gate insulating films covering a channel region between said source and intermediate regions and a channel region between said drain and intermediate regions;

a first film covering said source, drain and intermediate regions and made of insulating material, said first film being thicker than said gate insulating films;

a carrier trap film formed on each of the gate insulating films and made of material easier to trap carriers than said gate insulating films;

a coating film made of insulating material and covering a surface of each of said carrier trap films; and

a gate electrode covering said coating film and first film disposed in an area from one of the channel regions to the other of the channel regions via the intermediate region.

16. A semiconductor device according to claim 15, wherein said carrier trap film on one of said gate insulating films and said carrier trap film on the other of said gate insulating films are made continuous via a portion on said first film on said intermediate region.

17. A semiconductor device comprising:

a semiconductor substrate;

a plurality of impurity doped regions of a first conductivity type formed in a surface layer of said semiconductor substrate, extending in a first

direction and disposed in parallel to each other;

a plurality of gate lines disposed on or over said semiconductor substrate, extending in a second direction crossing the first direction and disposed in parallel to each other at some interval, said gate line being insulated from said impurity doped region at each cross point between said gate line and said impurity doped region; and

a FET disposed at each cross point between a pair of adjacent impurity doped regions and said gate line,

wherein each of said FET's comprises:

an intermediate region formed in the substrate surface layer between a corresponding pair of impurity doped regions and spaced apart by some distance from both the impurity doped regions, said intermediate region having the same conductivity type as the impurity doped regions;

gate insulating films covering channel regions between each of the impurity doped regions and said intermediate region;

a first film covering the pair of impurity doped regions and said intermediate region and made of insulating material, said first film being thicker than said gate insulating films;

a carrier trap film formed on each of the gate insulating films and made of material easier to trap carriers than said gate insulating films; and

a coating film made of insulating material and covering a surface of each of said carrier trap films,

wherein:

said gate line corresponding to respective FET's is disposed on said coating film and first film and serves also as gate electrodes of FET's; and

the semiconductor device further comprises a channel stopper

region of a second conductivity type opposite to the first conductivity type, said channel stopper region being formed in the substrate surface layer between channel regions of two FET's juxtaposed in the first direction.

18. A semiconductor device according to claim 17, wherein in each FET, said carrier trap film on one of said gate insulating films and said carrier trap film on the other of said gate insulating films are made continuous via a portion on said first film on said intermediate region.

19. A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a gate insulating film, a carrier trap film made of material easier to trap carriers than the gate insulating film, and an upper insulating film on a surface of a semiconductor substrate;

forming resist patterns on the upper insulating film, the resist patterns covering a pair of elongated areas disposed in parallel to each other and spaced apart from each other by some distance;

etching the upper insulating film and carrier trap film by using the resist patterns as a mask;

implanting impurity ions into a surface layer of the semiconductor substrate by using the resist patterns as a mask;

removing the resist patterns;

forming a first film made of insulating material in the surface layer of the semiconductor substrate in the area implanted with ions by said impurity ion implanting step; and

forming a gate electrode on the upper insulating films and the first

film between the upper insulating films.

20. A method according to claim 19, wherein the semiconductor substrate is a silicon substrate, and in said first film forming step, the first film is formed by locally oxidizing a surface layer of the semiconductor substrate by using the carrier trap films as a mask.

21. A method of manufacturing a semiconductor device comprising the steps of:

covering a pair of elongated areas disposed in parallel to each other and spaced apart from each other by some distance on a surface of a semiconductor substrate made of silicon, with resist patterns;

implanting impurity ions into a surface layer of the semiconductor substrate by using the resist patterns as a mask;

oxidizing the surface layer of the semiconductor substrate to form a first film of silicon oxide on a surface of an area where impurity ions were implanted and to form gate insulating films thinner than the first film on a surface of an area where impurity ions are not implanted;

sequentially forming a carrier trap film made of material easier to trap carriers than the gate insulating film and an upper insulating film on the first film and gate insulating film; and

forming a gate electrode on a surface of the upper insulating film in an area on or over at least the gate insulating films and the first film between the gate insulating films.